Notice of Allowability	Application No. 09/659,735	Applicant(s) SASAKI ET AL.	
	Examiner Hugh Jones	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/11/2000*.

2. ☒ The allowed claim(s) is/are *3-29*.

3. ☒ The drawings filed on *9/11/2000* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/11/2000
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. **Claims 3-29 of U. S. Application 09/659,735 filed on 9/11/2000, are presented for examination.** Claims 3-29 are allowed.

Allowable Subject Matter

2. Claims 3-29 are allowed over the prior art of record.

3. The following is an examiner's statement of reasons for allowance.

4. A prior art search has been carried out. The closest art of record is:

- **Berkelaar et al.** disclose the mapping problem for **pass transistor** selector mapping. **Pass transistor synthesis** is potentially important for semi-or full-custom design techniques. **Pass transistors** have the advantage that fewer transistors are needed, and that circuits with high fanin and small delay can be constructed. They present a an algorithm to address this problem, which is based an the idea of a general Boolean Oracle. The oracle is based on ATPG techniques, and compared to BDDs, the oracle has the advantage that failure to complete only affects optimization locally, and does not hinder optimization elsewhere in the logic. A limitation of BDDs is that it is difficult to complete the algorithm if a **BDD** grows too large.

- **Kumashiro et al.** disclose a given logic circuit which is divided into a combinational circuit portion and a register portion. The combinational circuit portion obtained by division is divided into a plurality of partial circuits having high connectivity. Each partial circuit is converted into a circuit having the transistor level. Then, a layout cell of the partial circuit having the transistor level is generated. Thereafter, arrangement and wiring are performed by using, as unit cells, a layout cell which corresponds to each register included in the register portion and the layout cell for each partial circuit in the combinational circuit so that a block layout is created. Accordingly, a layout having excellent characteristics can be created by a few kinds of cells in both circuits having the CMOS logic and the pass-transistor logic. In particular, the partial circuits having high connectivity are arranged in a cell in the circuit using the pass-transistor logic.

5. However, the prior art of record, while disclosing synthesis of logic circuits, including pass transistor circuits, with the use of binary decision diagrams, does not disclose or suggest the last limitation of the independent claims, namely:

"wherein said another partial diagram comprises one node which is used instead of said plurality of nodes, and a plurality of nodes which generate logical combination of a plurality of control variables each supplied to one

of said plurality of nodes included in said one partial diagram, and supplies said logical combination to said one node as a control variable,"

in the context of the claims.

6. Therefore, claims 3-29 are allowed over the prior art of record.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to: Dr. Hugh Jones telephone number (703) 305-0023, Monday-Thursday 0830 to 0700 ET, ***or*** the examiner's supervisor, Kevin Teska, telephone number (703) 305-9704. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to: Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to: (703) 308-9051 (for formal communications intended for entry) ***or***

(703) 308-1396 (for informal or draft communications, please label *PROPOSED* or *DRAFT*).

Dr. Hugh Jones

Primary Patent Examiner

September 4, 2004

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100